CLAIMS

1. An active matrix electroluminescent display device comprising an array of display pixels arranged in rows and columns, each pixel comprising:

an electroluminescent (EL) display element (2);

a drive transistor (24) for driving a current through the display element (2);

means (28) for interrupting the drive of current through the display element; and

row driver circuitry (8) for generating control voltages to be applied to the pixels in each row in sequence including a drive voltage for the interrupting means,

wherein the row driver circuitry comprises a shift register arrangement (50) and logic arrangement (52,54) for generating the drive voltage for the interrupting means (28), the drive voltage for the interrupting means including a pulse having a duration which can be varied up to substantially the full field period less the address period, wherein the signal or signals propagated through the shift register arrangement (50) control the pulse duration.

2. A device as claimed in claim 1, wherein the shift register arrangement and logic arrangement comprises first and second shift register devices (50), each having a pulse propagating through them, and logic means (54) for deriving a signal having a pulse with duration derived from the difference in timing of the pulses propagating through the first and second shift register devices (50).

3. A device as claimed in claim 2, wherein the pulse propagating in each shift register device (50) has a duration corresponding the line time of the display.

4. A device as claimed in claim 2 or 3, wherein the logic means comprises a transmission gate (60) which transmits a low pulse in response to

a pulse on one of the shift register devices and transmits a high pulse in response to a pulse on the other one of the shift register devices.

5. A device as claimed in claim 4, wherein the logic means further comprises a memory cell (62) for maintaining a constant output between pulses received from the transmission gate.

6. A device as claimed in claim 1, wherein the shift register arrangement and logic arrangement comprises first and second shift register devices (50), each having a pulse propagating through them, and logic means for deriving a signal having a pulse with duration derived from the duration of the pulse in one of the first and second shift register devices.

7. A device as claimed in claim 6, wherein the pulse propagating in one shift register device has a duration corresponding to the line time of the display and the pulse propagating in the other shift register device has a duration for controlling the display element (2) illumination period.

8. A device as claimed in claim 1, wherein the shift register arrangement and logic arrangement comprises a shift register device, having a pulse propagating through it having a duration dependent on the desired illumination time of the display element, and logic means (90) for deriving from the shift register device a pulse having a duration corresponding to the line time of the display.

9. A device as claimed in claim 8, wherein the logic means (90) for deriving from the shift register device a pulse having a duration corresponding to the line time of the display comprises a combination element for combining the pulse at the output of one shift register element (n) for one row with the pulse at the output of another shift register element (n+1) for an adjacent row.

10. A device as claimed in any preceding claim, wherein a first pulse from the shift register arrangement and logic arrangement is combined with a first template control signal or signals (A1, A2) to provide a first control signal or signals (A1r,A2r) for the addressing of the pixel, and a second pulse from the shift register arrangement and logic arrangement is combined with a second template control signal (A3) to provide the drive voltage (A3r) for the interrupting means both during the addressing of the pixel and during subsequent driving of the pixel.

11. A device as claimed in claim 10, wherein the first pulse has duration equal to the line time.

12. A device as claimed in claim 10 or 11, wherein the second pulse has duration selected to control the display element illumination time.

13. A device as claimed in any preceding claim, wherein each pixel comprises drive transistor threshold compensation circuitry (20, 22, 26).

14. A device as claimed in claim 13, wherein the drive transistor threshold compensation circuitry comprises first and second capacitors (20, 22) connected in series between the gate and source of the drive transistor (24), a data input to the pixel being provided to the junction between the first and second capacitors (20, 22) thereby to charge the first capacitor (20) to a voltage derived from the pixel data voltage, and a voltage derived from the drive transistor threshold voltage being stored on the second capacitor (22).

15. A device as claimed in claim 13 or 14, wherein the drive transistor (24), the electroluminescent display element (2) and means for interrupting (28) the drive of current through the display element are connected in series between a power supply line (30) and a common potential line.

16. A device as claimed in claim 15, wherein the means for interrupting (28) comprises a transistor.

17. A method of driving an active matrix electroluminescent display device comprising an array of display pixels arranged in rows and columns, in which each pixel comprises an electroluminescent (EL) display element (2), a drive transistor (24) for driving a current through the display element and means (28) for interrupting the drive of current through the display element, the method comprising:

propagating a pulse or pulses through a shift register arrangement (50);

using a pulse from the shift register arrangement (50) to allow pixel addressing control voltages to be applied to the pixels of a row during an addressing period;

using the shift register pulse or pulses to derive a drive voltage for the interrupting means (28) including a pulse having a duration which can be varied up to substantially the full field period less the addressing period; and

applying the drive voltage for the interrupting means to the interrupting means after the pixel addressing period.